AMENDMENT TO THE CLAIMS

1. (Currently amended) A method for fabricating a semiconductor device, comprising:

a first step of implanting, into a channel formation region of a semiconductor substrate, first dopant ions of a first conductivity type which are indium ions to form a dopant implantation layer in the channel formation region;

a second step of implanting second dopant ions into the semiconductor substrate to form [[an]] a first amorphous layer ~~expanding from the substrate surface to a region of the substrate deeper than the dopant implantation layer~~;

after the first and second steps, a third step of performing a first thermal treatment to diffuse the first dopant ions from the dopant implantation layer, thereby forming a first diffused layer of the first conductivity type in the channel formation region; and

after the third step, a fourth step of selectively forming a gate insulating film on the semiconductor substrate and a gate electrode on the gate insulating film,

wherein the first amorphous layer expands from the substrate surface to a region of the substrate deeper than the dopant implantation layer.

2. (Original) The method of claim 1, wherein the semiconductor substrate is made of silicon, and the second dopant ion belongs to group IV elements.

3. (Original) The method of claim 2, wherein the plane orientation of the semiconductor substrate is the {100} plane.

4. (Original) The method of claim 2, wherein the semiconductor substrate includes, in

the upper portion thereof, an epitaxial layer formed by epitaxially growing silicon.

5. (Original) The method of claim 2, wherein the semiconductor substrate includes, in the upper portion thereof, a strained silicon layer having a crystal lattice of a larger lattice constant than a normal lattice constant.

6. (Cancelled)

7. (Previously presented) The method of claim 1, wherein the dose of the indium ions to be implanted is 5×10^{13} /cm^2 or more.

8. (Previously presented) The method of claim 1, further comprising, after the fourth step,

a fifth step of implanting third dopant ions of a second conductivity type into the semiconductor substrate using the gate electrode as a mask, and

a sixth step of performing a second thermal treatment on the semiconductor substrate to diffuse the third dopant ions, thereby forming a second diffused layer of the second conductivity type.

9. (Previously presented) The method of claim 1, wherein the first thermal treatment is rapid thermal annealing performed at a heating rate of about 100°C/sec or higher, at a heating temperature of 850 to 1050°C, and either with the peak temperature of the treatment kept for 10 seconds at the maximum or with the peak temperature not kept.

10. (Currently amended) The method of claim 1, further comprising, ~~between the second and third steps~~ after the first and second steps and before the third step, the step of performing a third thermal treatment at such a temperature that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions.

11. (Original) The method of claim 10, wherein the heating temperature of the third thermal treatment is 400 to 600°C.

12. (Original) The method of claim 11, wherein the heating time of the third thermal treatment is 1 to 20 hours.

13. (Original) The method of claim 8, further comprising, between the fourth and sixth steps, the step of implanting fourth dopant ions of the first conductivity type into the semiconductor substrate using the gate electrode as a mask,

wherein the second thermal treatment performed in the sixth step diffuses the fourth dopant ions, thereby forming a third diffused layer of the first conductivity type below the second diffused layer.

14. (Original) The method of claim 8, further comprising, after the sixth step,

the step of forming sidewalls of an insulating film on the side surfaces of the gate electrode, and

the step of implanting fifth dopant ions of the second conductivity type into the

semiconductor substrate using the gate electrode and the sidewalls as a mask and then performing a fourth thermal treatment to diffuse the fifth dopant ions, thereby forming, outside the second diffused layer, a fourth diffused layer of the second conductivity type which has a deeper junction interface than the second diffused layer.

15-17. (Canceled)

18. (Previously presented) The method of claim 8, wherein the second step is performed after the first step.

19. (New) The method of claim 1,

wherein the second dopant ions is germanium ions.

20. (New) The method of claim 1,

wherein in the first step, the implantation of the first dopant ions containing indium ions forms, on the semiconductor substrate, a second amorphous layer which is shallower than the first amorphous layer.

21. (New) The method of claim 1,

wherein in the first step, the implantation of the first dopant ions containing indium ions forms an amorphous-crystal interface immediately below the region of the semiconductor substrate at which a dopant concentration of indium reaches the peak.

22. (New) The method of claim 21,

wherein the second dopant ions is germanium ions, and

in the second step, the implantation of germanium ions transfers the amorphous-crystal interface to the position in the semiconductor substrate deeper than the peak position of the dopant concentration of germanium.

23. (New) The method of claim 1,

wherein the first diffused layer is a diffused channel layer.

24. (New) The method of claim 1,

wherein the first thermal treatment in the third step restores the amorphous layer to a crystal layer.

25. (New) The method of claim 1,

wherein the second dopant ions is germanium ions,

the first diffused layer is a diffused channel layer, and

in the fourth step, an interface between the gate insulating film and the semiconductor substrate has a higher dopant concentration of germanium than a below side of the channel diffused layer.

26. (New) The method of claim 1,

wherein the second dopant ions is germanium ions,

the first diffused layer is a diffused channel layer, and

in the fourth step, a dopant concentration of germanium contained in an interface between the gate insulating film and the semiconductor substrate is about $5x10^{18}$ to $5x10^{21}$ atoms/cm^3 and the dopant concentration of germanium contained in the deeper side of the diffused channel layer is about $1x10^{15}$ to $1x10^{17}$ atoms/cm^3.

27. (New) The method of claim 1,

wherein the second dopant ions is germanium ions,

the first diffused layer is a diffused channel layer, and

in the fourth step, a region of the diffused channel layer slightly deeper than a surface of the semiconductor substrate has a higher dopant concentration of indium than the surface of the semiconductor substrate.

28. (New) The method of claim 1,

wherein the first thermal treatment is performed using laser annealing.

29. (New) The method of claim 1,

wherein the first thermal treatment is performed using flash annealing.

30. (New) The method of claim 1,

wherein the first step is performed after the second step.

31. (New) The method of claim 1,

wherein the first step is performed after the second step, and

the first thermal treatment is performed using laser annealing.

32. (New) The method of claim 1,

wherein the second dopant ions is germanium ions,

the first thermal treatment is performed using laser annealing.

33. (New) The method of claim 1,

wherein the first step is performed after the second step,

the second dopant ions is germanium ions, and

the first thermal treatment is performed using laser annealing.

34. (New) The method of claim 1,

wherein the first step is performed after the second step,

the second dopant ions is germanium ions, and

the first thermal treatment is performed using flash annealing.

35. (New) The method of claim 1,

wherein after the first and second steps and before the third step, a third thermal treatment is performed at a temperature of 400 to 600°C to the semiconductor substrate,

the second dopant ions is germanium ions, and

the first thermal treatment is performed using laser annealing.

36. (New) The method of claim 1,

wherein the first step is performed after the second step,

after the first step and before the third step, a fifth thermal treatment is performed at a temperature of 400 to 600°C to the semiconductor substrate,

the second dopant ions is germanium ions, and

the first thermal treatment is performed using laser annealing.

37. (New) The method of claim 1,

wherein after the first and second steps and before the third step, a third thermal treatment is performed at a temperature of 400 to 600°C to the semiconductor substrate,

the second dopant ions is germanium ions, and

the first thermal treatment is performed using flash annealing.